Wafer level fan-out packaging process

Publication number:	TW531854B
Publication date:	2003-05-11
Inventor:	YANG WEN-KUEN (TW); YANG WEN-BIN (TW)
Applicant:	ADVANCED CHIP ENGINEERING TECH (TW)
Classification:	
- International:	***H01L23/02;*** **H01L23/02;** (IPC1-7): H01L23/02
- european:	
Application number:	TW20010123655 20010925
Priority number(s):	TW20010123655 20010925

Abstract of **TW531854B**

The present invention is a semiconductor packaging technology, especially relating to a method of wafer level fan-out packaging process. The present invention comprises selecting the die after dicing, gluing the die on the glass base, and the I/O connector of metal pad glued on the die is processed through a special material/way, i.e. the position of I/O connector is extended in the way of fan-out so that the contact point is extended into the die edge and even the exterior of die, the fan-out of contact point has a larger range to implant the I/O implanted ball, therefore, the number of I/O implanted ball is increased to add more I/O contact points, and also the problems of signal coupling due to too close pitch and solder bridge due to too close solder connector are decreased. The characteristic of the present invention is to use the original packaging machine without additional cost. At the same time, the present invention can be applied to the 8 inch and 12 inch packaging process, and comprises die, capacitor and multi-chip or plural passive devices, such as CPU, DRAM, SRAM packaging processes on the packaging base. In addition, since the base selected is glass base, the unbalanced stress problem due to different materials used between different layers do not occur, so as to enhance the reliability.
